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19-0889; Rev 1; 7/96

MAXIM

CMOS High Speed 8-Bit A/D Converter with Track/Hold Function

ADC0820

General Description

The ADC0820 is a high speed, microprocessor compatible, 8 bit analog-to-digital converter which uses a half-flash technique to achieve a conversion time of 1.4 µs. The converter has a 0V to +5V analog input range and uses a single +5V supply.

A built-in track-and-hold function is included, eliminating the need for an external track-and-hold for input slew rates up to 100mV/µs.

The A/D easily interfaces with microprocessors by appearing as a memory location or I/O port without the need for external interfacing logic. Data outputs use latched, three-state buffer circuitry to allow direct connection to a microprocessor data bus or system I/O port. An over-flow output is also provided for cascading devices to achieve higher resolution.

Maxim's ADC0820 is pin-compatible with National Semiconductor's ADC0820 and provides improved specifications. It is packaged in 20-pin Small Outline, DIP and CERDIP packages.

Applications

Digital Signal Processing
High Speed Data Acquisition
Telecommunications
High Speed Servo Loops
Audio Systems

Features

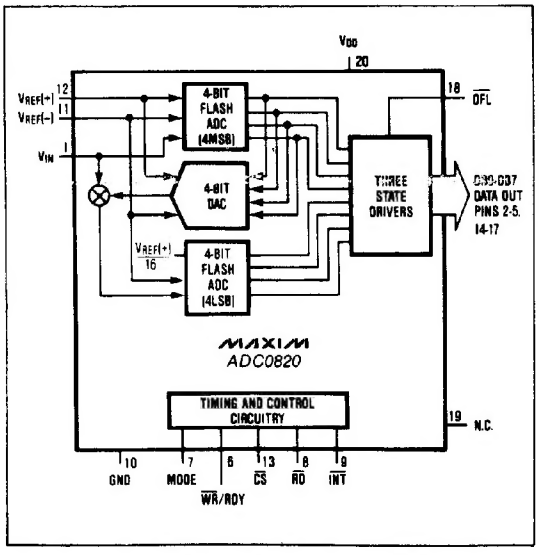
- ◆ **Fast Conversion Time: 1.4µs Max.**
- ◆ **Built-in Track-and-Hold Function**
- ◆ **No Missing Codes**
- ◆ **No User Adjustments Required**
- ◆ **Single +5V Supply**
- ◆ **No External Clock**
- ◆ **Easy Interface To Microprocessors**

Ordering Information

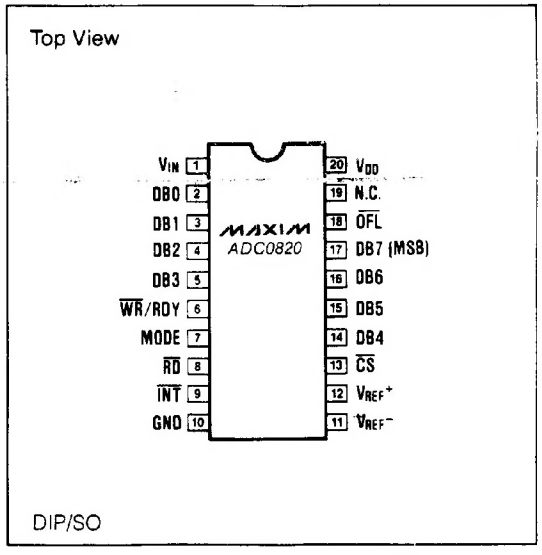
PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
ADC0820BCN	0° C to +70° C	20 Plastic DIP	±1/2
ADC0820CCN	0° C to +70° C	20 Plastic DIP	±1
ADC0820CC/D	0° C to +70° C	Dice*	±1
ADC0820BCM	0° C to +70° C	20 SO	±1/2
ADC0820CCM	0° C to +70° C	20 SO	±1/2
ADC0820BCJ	-40° C to +85° C	20 CERDIP	±1/2
ADC0820CCJ	-40° C to +85° C	20 CERDIP	±1
ADC0820BJ	-55° C to +125° C	20 CERDIP**	±1/2
ADC0820CJ	-55° C to +125° C	20 CERDIP**	±1

*Dice are specified at T_A = +25°C.
**Contact factory

Functional Block Diagram



Pin Configuration



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CMOS High Speed 8-Bit A/D Converter with Track/Hold Function

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} to GND ..... 0V, +10V
Voltage at any other pins
(Pins 1-9, 11-19) ..... GND - 0.3V, V_{DD} +0.3V
Output current (Pin 19) 30mA
Power Dissipation (Any Package) to +75°C 450mW
Derate Above +25°C by ..... 6mW/°C

Operating Temperature Ranges
ADC0820BC_/CC_ ..... 0°C to +70°C
ADC0820BCJ/CCJ ..... -40°C to +85°C
ADC08020BJ/CJ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, RD-MODE, T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
ACCURACY						
Resolution			8			bits
Total Unadjusted Error (Note 1)		ADC0820B ADC0820C			±1/2 ±1	LSB
No Missing Codes Resolution			8			bits
REFERENCE INPUT						
Reference Resistance		T_A = +25°C T_A = T_{MIN} to T_{MAX}	1.4 1.25	2.2	4.0 4.0	kΩ
V_{REF}^+ Input Voltage Range			V_{REF}^-		V_{DD} + 0.1	V
V_{REF}^- Input Voltage Range			GND - 0.1		V_{REF}^+	V
ANALOG INPUT						
Analog Input Voltage Range	V_{INR}		GND - 0.1		V_{DD} + 0.1	V
Analog Input Capacitance	C_{VIN}			45		pF
Analog Input Current	I_{VIN}	V_{IN} = 0V to +5V; T_A = +25°C, T_{MIN} to T_{MAX}			±0.3 ±3	μA
Slew Rate, Tracking (Note 2)	SR			0.2	0.1	V/μs
LOGIC INPUTS						
Input HIGH Voltage	V_{INH}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$ MODE	2.0 3.5			V
Input LOW Voltage	V_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$ MODE			0.8 1.5	V
Input High Current	I_{INH}	$\overline{CS}$, $\overline{RD}$; T_A = +25°C, T_{MIN} to T_{MAX}			0.1 1	μA
		$\overline{WR}$; T_A = +25°C, T_{MIN} to T_{MAX}			0.3 3	
		MODE; T_A = +25°C, T_{MIN} to T_{MAX}		50	150 200	
Input Low Current	I_{INL}	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, MODE; T_A = 25°C, T_{MIN} to T_{MAX}			-0.3 -1	μA
Input Capacitance (Note 3)	C_{IN}	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, MODE		5	8	pF
LOGIC OUTPUTS						
Output HIGH Voltage	V_{OH}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$ V_{DD} = +4.75V, I_{OUT} = -360μA V_{DD} = +4.75V, I_{OUT} = -10μA	4.0 4.5			V
Output LOW Voltage	V_{OL}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$, RDY V_{DD} = +4.75V, I_{OUT} = 1.6mA			0.4	V
Three-state Output Current		DB0-DB7, RDY; T_A = +25°C, T_{MIN} to T_{MAX}	-0.3 -3		+0.3 +3	μA
Output Capacitance (Note 3)	C_{OUT}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$, RDY		5	8	pF
Output Source Current	I_{SRC}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$; V_{OUT} = 0		-25	-10	mA
Output Sink Current	I_{SINK}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$, RDY; V_{OUT} = V_{DD}		40	15	mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, RD-MODE, T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
POWER SUPPLY						
Supply Voltage	V_{DD}	±5% for Specified Performance		5		V
Supply Current	I_{DD}	$\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = 0 T_A = +25°C T_{MIN} to T_{MAX}		5	10 15	mA
Power Dissipation		$\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = 0		25		mW
Power Supply Sensitivity	PSS	V_{DD} = ±5%		±1/16	±1/4	LSB

TIMING CHARACTERISTICS

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, T_A = T_{MIN} to T_{MAX}, unless otherwise specified. See Note 2, 4.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			ADC0820BCX ADC0820CCX		ADC0820BJ ADC0820CJ		UNITS
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Setup Time	t_{CSS}		0			0		0		ns
$\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Hold Time	t_{CSH}		0			0		0		ns
$\overline{CS}$ to RDY Delay	t_{RDY}	C_L = 50pF, R = 3kΩ		35	70		90		100	ns
Conversion Time (RD Mode)	t_{CRD}	(Note 7)		1.2	1.6		2.0		2.5	µs
Data Access Time (RD Mode) (See Figure 1)	t_{ACC0}	(Note 5)		t_{CRD} + 10	t_{CRD} + 35		t_{CRD} + 50		t_{CRD} + 70	ns
$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)	t_{INTH}	C_L = 50pF		60	125		175		225	ns
Data Hold Time	t_{DH}	(Note 6)		40	90		120		150	ns
Delay Time Between Conversions	t_P		500			600		600		ns
Write Pulse Width	t_{WR}		600		50,000	600	50,000	600	50,000	ns
Conversion Time (WR-RD Mode)	t_{CWR-RD}		1.4			1.56		1.62		µs
Delay between $\overline{WR}$ and $\overline{RD}$ Pulses	t_{RD}		600			700		700		ns
Data Access Time (WR-RD Mode) (See Figure 3)	t_{ACC1}	$t_{RD} < t_{INTL}$		110	220		280		350	ns
$\overline{RD}$ to $\overline{INT}$ Delay	t_{RI}			100	200		260		320	ns
$\overline{WR}$ to $\overline{INT}$ Delay	t_{INTL}			600	1000		1400		1700	ns
Data Access Time (WR-RD Mode) (See Figure 2)	t_{ACC2}	$t_{RD} > t_{INTL}$, (Note 6)		60	100		130		160	ns
$\overline{WR}$ to $\overline{INT}$ Delay (Stand-Alone)	t_{IHWR}	C_L = 50pF		70	100		130		150	ns
Data Access Time After $\overline{INT}$	t_{ID}			10	50		65		75	ns

Note 1: Total unadjusted error includes offset, full-scale and linearity errors.
Note 2: Sample tested at +25°C by Quality Assurance to ensure compliance.
Note 3: Guaranteed by design.
Note 4: All input control signals are specified with t_R = t_F = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
Note 5: Defined as the time required for an output to cross 0.8V or 2.4 V.
Note 6: Defined as the time required for the data lines to change 0.5V.
Note 7: For faster conversions use WR-RD Mode.

CMOS High Speed A/D Converter with Track/Hold Function

Pin Description

PIN	NAME	FUNCTION
1	V_{IN}	Analog input: range = GND < V_{IN} < V_{DD}.
2	DB0	Three-state data output, bit 0 (LSB).
3	DB1	Three-state data output, bit 1.
4	DB2	Three-state data output, bit 2.
5	DB3	Three-state data output, bit 3.
6	$\overline{WR}$/RDY	WRITE control input/READY status output. See Digital Interface section.
7	MODE	Mode selection input. This input is internally pulled low with a 50μA current source. RD Mode: MODE low/open. WR-RD Mode: MODE high.
8	$\overline{RD}$	READ input. $\overline{RD}$ must be low to access data. See Digital Interface section.
9	$\overline{INT}$	INTERRUPT output. $\overline{INT}$ going low indicates the completion of a conversion. See Digital Interface section.
10	GND	Ground.
11	V_{REF}^-	Lower limit of reference span. Sets the zero code voltage. Range: GND to V_{REF}^+.
12	V_{REF}^+	Upper limit of reference span. Sets the Full Scale input voltage. Range: V_{REF}^- to V_{DD}.
13	$\overline{CS}$	CHIP-SELECT input. $\overline{CS}$ must be low for the device to recognize $\overline{WR}$ or $\overline{RD}$ inputs
14	DB4	Three-state data output, bit 4.
15	DB5	Three-state data output, bit 5.
16	DB6	Three-state data output, bit 6.
17	DB7	Three-state data output, bit 7 (MSB).
18	$\overline{OFL}$	Overflow Output. If the analog input is greater than V_{REF}^+, $\overline{OFL}$ will be high at the end of the conversion. It can be used to cascade two or more devices to increase resolution.
19	N.C.	Test Pin. Do not connect.
20	V_{DD}	Power supply voltage, +5V.

Digital Interface

RD Mode (Pin 7 Low)

A conversion is started by taking $\overline{RD}$ low and keeping it low until output data appears (Figure 1). Pin 6 ($\overline{WR}$/RDY) is configured as a status output (RDY) in this mode, and is used with microprocessors which can be forced into a WAIT state. The processor starts a conversion, waits, and then reads data with a single READ instruction. RDY, an open collector output, goes low after the falling edge of $\overline{CS}$ and goes high impedance at the end of the conversion. $\overline{INT}$ goes low at the end of the conversion and returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

WR-RD Mode (Pin 7 High)

In the WR-RD mode, pin 6 ($\overline{WR}$/RDY) is the WRITE input for the converter. With $\overline{CS}$ low, a conversion starts on the falling edge of $\overline{WR}$. There are several options for reading data:

Using the Internal Delay

The processor waits for $\overline{INT}$ to go low before reading data (Figure 2). $\overline{INT}$ typically goes low 600ns after the rising edge of $\overline{WR}$, indicating that the conversion is complete. With $\overline{CS}$ low, DB0-DB7 are read by pulling $\overline{RD}$ low. $\overline{INT}$ is then reset on the rising edge of $\overline{CS}$ or $\overline{RD}$.

Reading Before Delay

The conversion time is externally controlled with $\overline{RD}$ (Figure 3). The status of $\overline{INT}$ is ignored and $\overline{RD}$ is taken low as soon as 600ns after the rising edge of $\overline{WR}$. This completes the conversion and enables DB0-DB7. $\overline{INT}$ goes low after the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$.

Pipelined Operation

"Pipelined" operation is achieved by tying $\overline{WR}$ and $\overline{RD}$ together (Figure 4). With $\overline{CS}$ low, taking $\overline{WR}$ and $\overline{RD}$ low starts a new conversion and, at the same time, reads the result of the previous conversion.

Stand-Alone Operation

In stand-alone operation, $\overline{CS}$ and $\overline{RD}$ are tied low and a conversion is initiated by pulling $\overline{WR}$ low (Figure 5). Output data is valid approximately 600ns after the rising edge of $\overline{WR}$.

Analog Considerations

Reference Input

The $V_{REF}(+)$ and $V_{REF}(-)$ inputs of the converter set the full-scale and zero input voltages. The voltage at $V_{REF}(-)$ defines the input level which produces an output code of all zeroes, and the voltage at $V_{REF}(+)$ defines the input which produces an output code of all ones (see Figure 6). Figure 7 shows some reference configurations.

Bypassing

A 47μF electrolytic and 0.1μF ceramic capacitor should be used to bypass the V_{DD} pin to GND. The lead length of these capacitors should be as short as possible. If the reference inputs (pins 11, 12) are driven by long lines, they also should be bypassed to GND with 0.1 μF capacitors at the reference input pins.

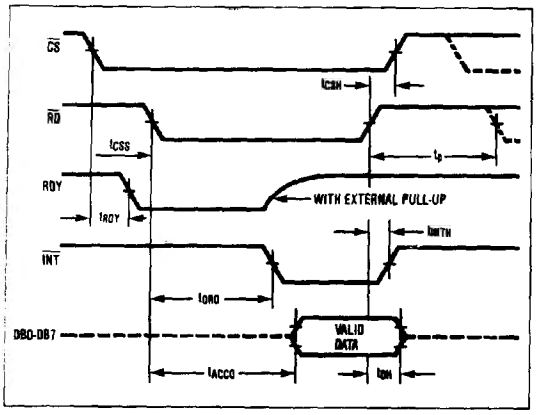


Figure 1. RD Mode Timing

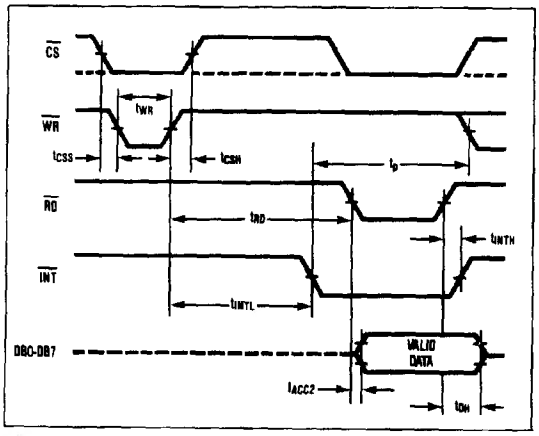


Figure 2. WR-RD Mode Timing ($t_{RD} > t_{INTL}$)

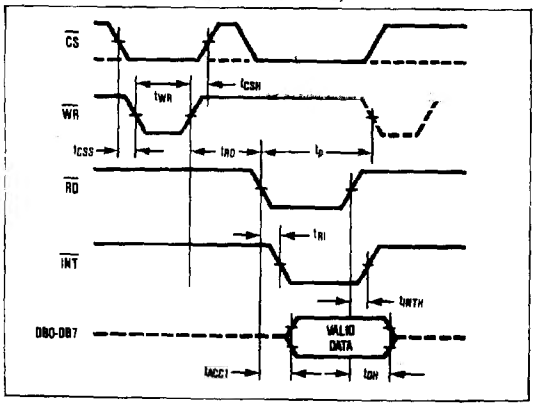


Figure 3. WR-RD Mode Timing ($t_{RD} < t_{INTL}$)

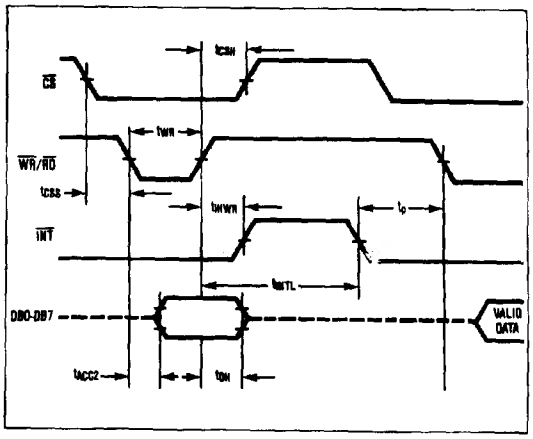


Figure 4. WR-RD Mode Pipe-Lined Timing, $\overline{WR} = \overline{RD}$

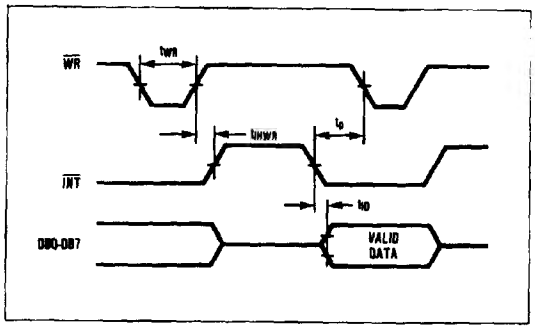


Figure 5. WR-RD Mode Stand-Alone Timing, $\overline{CS} = \overline{RD} = 0$

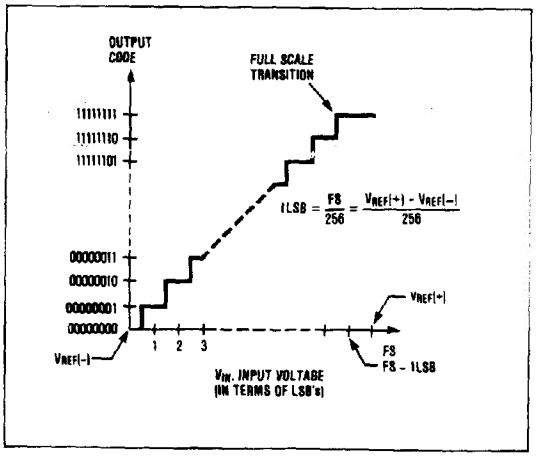


Figure 6. Transfer Function

CMOS High Speed A/D Converter with Track/Hold Function

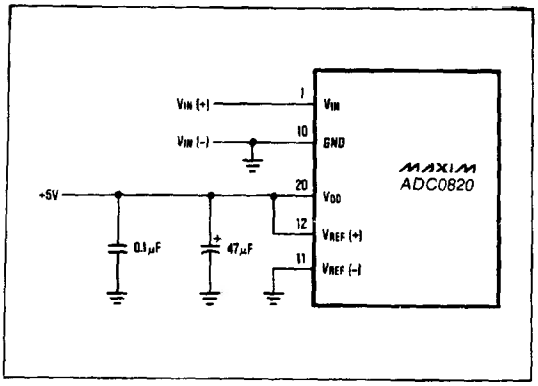


Figure 7a. Power Supply as Reference

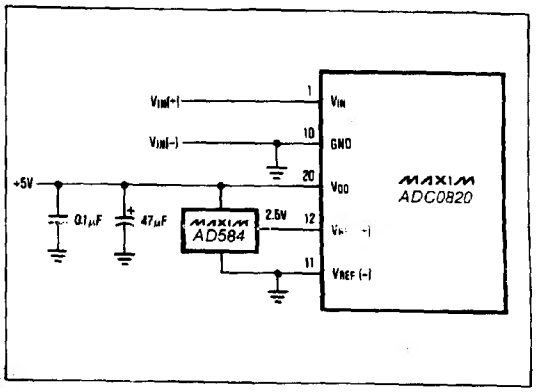


Figure 7b. External Reference 2.5V Full Scale

Input Current

The ADC0820 analog input behaves somewhat differently from conventional A/D converters. The ADC0820 takes varying amounts of current from the input depending on the operating cycle of the A/D.

During the input sampling phase ($\overline{WR}$ = LOW in the (WR-RD Mode) input capacitors must be charged to the input voltage through the resistance of internal analog switches (about 2kΩ to 5kΩ). In addition, about 12pF of stray capacitance (C_S) must be charged. An equivalent RC model of the input is shown in Figure 8. The 45pF input capacitance allows source resistances (R_S) of up to 1kΩ to be used without increased settling time. For larger resistances, the width of the $\overline{WR}$ pulse must be increased from 600ns. In the RD mode, where the sample time is fixed, R_S greater than 1kΩ may cause settling errors. In this case, use the WR-RD mode and greater than 600ns $\overline{RD}$ time, or use a buffer to drive the analog input.

Input Filtering

The ADC0820's sampled data comparators generate input transients at V_{IN}. This does not degrade performance since the A/D only "looks" at the input after these transients occur. It is not necessary to filter these transients with an external capacitor at the V_{IN} terminal.

Inherent Track-and-Hold

The ADC0820 can measure a variety of high speed input signals without the help of an external sample-and-hold. The input is tracked from the time $\overline{WR}$ goes low (in the WR-RD mode) to approximately 100ns after it returns high. Input signals with slew rates typically up to 200mV/µs can be converted without error.

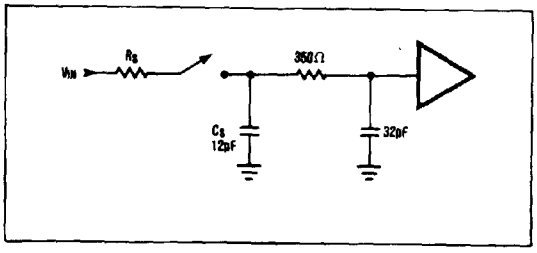
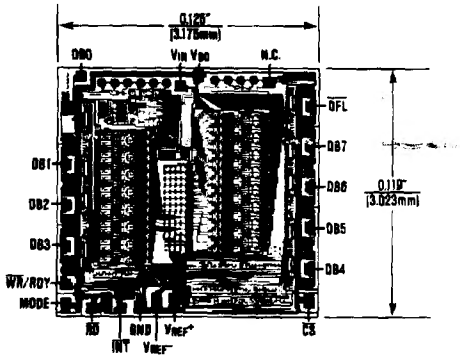


Figure 8. Equivalent Input Model

Chip Topography



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